In view of the foregoing amendments and following remarks responsive to the Office Action of March 26, 2004, Applicant respectfully requests favorable reconsideration of this Application.

Claim Rejections

The Office rejected claims 1–18 under 35 U.S.C. § 112, second paragraph, as being indefinite. The Office further rejected claims 1–3, 5, 6, 8–11, 13 and 14 as being anticipated by Bergmann et al. (U.S. Patent No. 4,821,297). The Office further rejected claims 4 and 12 under 35 U.S.C. § 103(a) as being unpatentable over Bergmann et al. in view of Stuart (U.S. Patent No. 3,746,800). Finally, the Office indicated that claims 7 and 15–18 would be allowable if rewritten to overcome the rejections under 35 U.S.C. § 112, second paragraph, and to include all of the limitations of the base claim and any intervening claims.

The Cited Art

Bergmann et al. discloses a digital clock recovery circuit developed by AT&T Bell Laboratories in Murray Hill in the 1980s. In that circuit, a reference clock is used to provide a plurality of N signals with different clock phases. The incoming data stream is sampled via a multi-tap delay line and latches that are clocked by the reference clock to generate a plurality of M samples for each data bit. The logic values of the M samples are then compared to determine the relationship between the current clock phase and

the data bit transition. In particular, if all samples agree, the clock phase is deemed to be correctly aligned with the data. If the clock phase is either leading or lagging the data, various samples will disagree. In the latter situation, the clock phase is incremented or decremented in accordance with a lookup table until all of the samples agree. The particular clock that provides this state is used as the recovered clock signal.

Stuart describes a still-earlier clock recovery circuit from the 1970s, in which a group of sample-and-hold flip-flops are used to "slice" and sample a data signal at four times the bit rate of the data signal. The samples are then passed to a combinational logic circuit for a determination as to whether the local clock phase should be incremented or decremented. The Office cited Stuart as teaching the use of bistable multi-vibrators as buffer components and as teaching the use of dual-rail amplifiers. (3/26/04 OA, p. 7).

The Present Invention

The present invention builds upon, but is distinguishable from, these earlier clock and data recovery circuits. Like these prior art circuits, the present invention is a clock and data recovery circuit that samples a data signal and adjusts the phase of a local clock based on the data signal samples. In the present invention, however, two important improvements have been made. First, the present invention makes use of an additional input to the phase selector circuit: namely, the sampled state of the data signal during the previous cycle. This input is included in the lookup table and used to

more reliably determine the position of the data signal with respect to the recovered

clock signal. Second, the present invention uses a novel timing for the three or more

samples: in the present invention, the second and third samples are 180 degrees out of

phase, plus or minus a parameter M, with respect to the first sample — i.e., they are

symmetrically distributed around the point that is 180 degrees out of phase from the first

sample. These two improvements yield a surprisingly stable alignment of the data and

clock signals in comparison with the prior art.

Claim Amendments

The application as filed included original claim sets 1–12 and 13–18. In the

present amendment, the Applicant has amended independent claims 1 and 13 to

incorporate the limitations of original dependent claims 6 and 7 and original dependent

claim 15, respectively, and has canceled claims 6, 7 and 15. Further, the Applicant has

made claims 16 and 18 independent by incorporating most, though not all, of the

limitations of their respective parent claims. Further, the Applicant has amended claims

1–2, 5, 8–11, 13–14 and 16–18 to remove certain claim limitations and to make

typographical corrections. The Applicant has also added new claims 19–28. New

independent claim 19 and dependent claims 20–27 incorporate most, though not all, of

the limitations of original claim 10 and its parent claims and the original claims 2–12.

New independent claim 28 corresponds to original claim 15 and includes most, though

not all, of its limitations, as further discussed below. These amendments and new

claims are described in more detail in the paragraphs that follow below.

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Discussion

The Office rejected claims 1–18 under 35 U.S.C. § 112, second paragraph, as being indefinite because the term "said clock phases" in claim 1, line 13 and the term "the clock phases" in claim 13, line 11 lack antecedent basis. The Office also rejected claim 8 because it recites the term "and/or." Applicant has amended the claims to provide suitable antecedent basis for the term "clock phases" in the claims, and amended claim 8 to eliminate the objectionable term. Applicant submits that the remaining claims are allowable under 35 U.S.C. § 112, second paragraph.

The Office further rejected claims 1–3, 5–6, 8–11, 13 and 14 as anticipated by Bergmann et al. (U.S. Patent No. 4,821,297) but indicated that claims 7 and 15–18 would be allowable if rewritten as discussed above. In the present amendment, the Applicant has amended independent claims 1 and 13 to incorporate the limitations of original dependent claims 6 and 7 and original dependent claim 15, respectively, and has canceled claims 6, 7 and 15.

In particular, claim 1 now recites the limitation formerly contained in claim 6 that the buffer component is "triggered by a first clock phase i, a second clock phase j and a third clock phase k, resulting in a buffering of the state of said data signal at said clock phases i, j, and k," as well as the limitation formerly contained in claim 7 that "the clock phases i, j, and k are related interdependent by at least one of the equations:

$$j = i + N/2 - M \text{ and } k = i + N/2 \text{ if } i \leq N/2 \text{ and}$$

$$j = i - N/2 - M \text{ and } k = i - N/2 + M \text{ if } i > N/2$$

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with a parameter M selectable within $0 < M < N/2$."

The Applicant notes, however, that the claim limitation contained in claim 5 concerning the "first, second, and third buffer portions" has not been imported into claim 1 and that the claim limitation in claim 1 concerning the counter has been relocated from claim 1 to dependent claim 2. The Applicant has further amended claim 1 to remove the limitation that "three or more of said clock phases are selected by said phase selector and the data sampling is triggered by said three or more clock phases." Applicant submits that claim 1 is allowable without these limitations. Applicant has further modified the limitations in claim 1 to clarify that either of the two identified equations relating clock phases i, j, and k are compatible with the present invention.

The Applicant has similarly amended claim 13 to add the limitations formerly contained in claim 15, that "the data signal is binary signal . . . and . . . is buffered by a first, a second, and a third group of bistable multivibrators . . . ," and accordingly canceled claim 15. As in claim 1, the Applicant has further amended claim 13 to remove the limitation that the phase selector "selects three or more of the clock phases and triggers the data sampling by said three or more clock phases" and relocated the limitation concerning the counter to dependant claim 14. The Applicant submits that claim 13 is allowable without these limitations.

Claims 2–3, 5, 8–11, and 14, which the Office rejected as anticipated by Bergmann et al., are allowable because they depend from amended claims 1 and 13 and are allowable for the same reasons as claims 1 and 13, discussed above.

The Office further rejected claims 4 and 12 under 35 U.S.C. § 103(a) as being unpatentable over Bergmann et al. in view of Stuart (U.S. Patent No. 3,746,800). The Applicant submits that these claims are allowable because they depend from amended claim 1 and are thus allowable for the same reasons as claim 1, discussed above.

With respect to claims 16–18, the Office indicated that these claims would be allowable if rewritten to overcome the rejections under 35 U.S.C. § 112, second paragraph, and to include all of the limitations of the base claim and any intervening claims. As discussed above, the Applicant has amended the claims to overcome the rejections under 35 U.S.C. § 112, and amended claims 16 and 18 to make them independent. In particular, claims 16 and 18 as amended now include all of the previously included limitations except the following three limitations: (1) the limitation formerly contained in claim 15 that the data signal be buffered by bistable multivibrators and (2) the limitation formerly contained in claim 13 concerning the counter, and (3) the limitation formerly contained in claim 13 that the phase selector "selects three or more of the clock phases and triggers the data sampling by said three or more clock phases."

Finally, minor typographical and grammatical corrections have also been made to claims 1–2, 5, 7–8, 11, 13, 14, and 16–18.

The Applicant has added new claims 19–28. New claim 19 corresponds to original claim 10 and includes its limitations and most of the limitations of its original parent claims 1, 5 and 9. Like the present claim 1, new claim 19 no longer includes the limitations concerning the counter and the limitation that "three or more of said clock phases are selected by said phase selector and the data sampling is triggered by said three or more clock phases." Because new claim 19 corresponds to original claim 10, the Office's rejection of original claim 10 as being anticipated by Bergmann et al. (U.S. Patent No. 4,821,297) is applicable to new claim 19. The Office asserts that Bergmann et al. anticipates the claimed invention, and in particular the limitation that "the phase detector further detects the signal state of the data signal at the clock phase i of the previous cycle of the timing signal." The Office asserts that the phase detector of Bergmann et al. "detects the signal state of the data signal (Bergmann fig. 1, col. 5 table shows signal state of data signal with RD1, RD2 and RD3) at the clock phase i (Bergmann fig. 1: output of 22) of the previous cycle of the timing signal (Bergmann fig. 1: three cycles of the timing signal as represented by DD1 or RD1, DD2 or RD2, DD3 or RD3 so anyone of the first two sets can be previous)."

The Applicant controverts the Office's rejection of original claim 10, now new claim 19. Applicant respectfully submits that the Office has read the teaching of Bergmann et al. too broadly. Bergmann et al. identifies signals DD1, DD2 and DD3 as "three separate waveforms . . . each a distinct, delayed representation of the input D." (Bergmann et al., col. 3, ll. 46-47). These signals DD1–DD3 are input to three latches,

and the outputs from the latches are "clocked logic values of these waveforms," defined as retimed data samples RD1, RD2, and RD3. (Id., col. 3, ll. 47-49). Signals DD1–DD3 and RD1–RD3 are further clarified in Figs. 2 and 3 of Bergmann et al., which depict RD1–RD3 (and by extension signals DD1–DD3) as falling within a one-period range (between, e.g., the striped lines of Fig. 2, or the solid lines of Fig. 3), rather than being taken from a "previous cycle of the timing signal" as required by new claim 19. Thus, Bergmann et al. fails to teach or suggest that "the phase detector further detects the signal state of the data signal at the clock phase i of the previous cycle of the timing signal" as set forth in new claim 19.

New claims 20–27 depend from claim 19 and are allowable for the same reasons as claim 19, discussed above.

New claim 28 is a system claim that corresponds to the presently amended claim 13. Like claim 13, claim 28 recites the limitation that the "data signal is buffered by a first, a second and a third group of bistable multivibrators . . . ." Claim 28 is thus allowable for the same reasons as claim 13.

In view of the foregoing amendments and remarks, this application is now in condition for allowance. Applicant respectfully requests the Examiner to issue a Notice of Allowance at the earliest date. The Examiner is invited to contact Applicant's undersigned counsel by telephone call in order to further the prosecution of this case in any way.

Respectfully submitted,

_7/26/04_
Dated

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